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09/823,929	03/31/2001	John T. Orchard	15685P076	7551

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,929	ORCHARD, JOHN T.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-5 and 7-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-5 and 7-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08/23/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 08/23/20004.

2. Claims 2-5 and 7-43 are pending in this application. Claims 2, 17, and 32 are pending in the application. In Amendment, claims 2, 5, 17, 20-21, and 32 are amended and claims 42-43 are added. This action is made final.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 2-5, 7-31, and 43 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 2, the term "maximally" in line 7 is a relative term which renders the claim indefinite. The term "maximally" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. For examination purposes, the examiner consider the term "maximally" is the best or highest number it can have. Claims 17 and 43 have the same rejection as above.

Re claim 5, the limitation "the atomic structure of a dedicated logic device" in lines 2-3 lacks an antecedence basis. For examination purposes, the examiner disregards

the limitation "the atomic structure of a dedicated logic device" in lines 2-3. Claim 20 has the same rejection as above.

Thus, claims 3-4, 7-16, 18-19, and 21-31 are also rejected for being dependent on the rejected base claims 2 and 5 respectively.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 2-3, 5, 7-9, 17-18, and 20-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Grisamore (U.S. 6,535,901).

Re claim 2, Grisamore discloses in Figures 1, 4-5, and 7 an apparatus comprising a plurality of inputs to receive multiple input terms (1st current multiplicand 20, 2nd current multiplicand 22, and partial product generator 12); a multi-stage series of Boolean function generators (14) coupled with the inputs to implement one or more full-adders, half-adders (col. 2 lines 36-40 and col. 3 lines 55-61), and single registers (col. 1 lines 36-38) to produce intermediate summation results (output of reduction tree module 14) by combining the input terms (partial product terms from generator 12) according to a pipelined reduction pattern (col. 2 lines 35-42), such that input bits of equal significance are maximally partitioned into groups of three to serve as inputs to full-adders (col. 8

lines 20-33), remaining groups of two to serve as inputs to half-adders (col. 8 lines 20-33), and remaining single bits to serve as inputs to single registers (col. 5 lines 48-53); and a multi-input adder (18) logically coupled with the series of Boolean function generators (14) to produce a final sum (34) of the input terms by combining the intermediate summation results (output of 14).

Re claim 3, Grisamore further discloses in Figures 1, 4-5, and 7 the input terms include one or more accumulator bits (26 and 28).

Re claim 5, Grisamore further discloses in Figures 1, 4-5, and 7 the Boolean function generator pairs with an associated register (16 and col. 1 lines 35-40) to form the atomic structure of a dedicated logic device.

Re claim 7, Grisamore further discloses in Figures 1, 4-5, and 7 the multi-input adder comprises an adder with an input for each single register in a final stage of the multiple stages of the series (18 and col.3 lines 60-63).

Re claim 8, Grisamore further discloses in Figures 1, 4-5, and 7 single registers in the series of Boolean function generators to receive feedback accumulator bits (26 and 28) from the multi-input adder, the accumulator bits resulting from a multiply-accumulate operation (output of 18).

Re claim 9, Grisamore further discloses in Figures 1, 4-5, and 7 single registers in the series of Boolean function generators to receive feedback accumulator bits from the multi-input adder, the accumulator bits resulting from a multiply-accumulate operation and an accumulator coupled with the multi-input adder to feed the accumulator bits back into the series of Boolean function generator (Figure 1).

Re claim 17, it is a method claim of claim 2. Thus, claim 17 is also rejected under the same rationale in the rejection of rejected claim 2.

Re claim 18, it is a method claim of claim 3. Thus, claim 18 is also rejected under the same rationale in the rejection of rejected claim 3.

Re claim 20, it is a method claim of claim 5. Thus, claim 20 is also rejected under the same rationale in the rejection of rejected claim 5.

Re claim 21, it is a method claim of claim 6. Thus, claim 21 is also rejected under the same rationale in the rejection of rejected claim 6.

Re claim 22, it is a method claim of claim 7. Thus, claim 22 is also rejected under the same rationale in the rejection of rejected claim 7.

Re claim 23, it is a method claim of claim 8. Thus, claim 23 is also rejected under the same rationale in the rejection of rejected claim 8.

Re claim 24, it is a method claim of claim 9. Thus, claim 24 is also rejected under the same rationale in the rejection of rejected claim 9.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4, 10-12, 19, and 25-27 are rejected under 35 U.S.C. 103(a) as being obvious over Grisamore (U.S. 6,535,901) in view of Chang et al. ("Hardware-efficient implementations for discrete function transforms using LUT-based FPGAs").

Re claim 4, Grisamore does not disclose the Boolean function generator comprise four-input look-up tables (LUTs) to implement Boolean logic functions. However, Chang et al. disclose in Figure 1(a) Boolean function generator comprise four-input look-up tables (LUTs) to implement Boolean logic functions (left column page 310 lines 1-5). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a LUTs to implement Boolean logic functions as seen in Chang's invention into Grisamore's invention because it would enable to reduce the hardware cost.

Re claims 10-12, Grisamore does not disclose in Figures 1, 4-5, and 7 the series of Boolean function generators is incorporated in a dedicated logic device comprising a FPGA wherein the device with control logic and a block of dedicated logic. However, Chang et al. disclose the series of Boolean function generators is incorporated in a dedicated logic device comprising a FPGA wherein the device with control logic and a block of dedicated logic (2nd paragraph on the left column page 309). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to implement the Boolean function generators in a dedicated logic device comprising a FPGA with control logic and a block of dedicated logic as seen in Chang et al.'s invention into Grisamore's invention because it would enable an operator to

dynamically program his/her own logic functions based on needs and cost (2nd paragraph on the left column page 309).

Re claim 19, it is a method claim of claim 4. Thus, claim 19 is also rejected under the same rationale in the rejection of rejected claim 4.

Re claim 25, it is a method claim of claim 10. Thus, claim 25 is also rejected under the same rationale in the rejection of rejected claim 10.

Re claim 26, it is a method claim of claim 11. Thus, claim 26 is also rejected under the same rationale in the rejection of rejected claim 11.

Re claim 27, it is a method claim of claim 12. Thus, claim 27 is also rejected under the same rationale in the rejection of rejected claim 12.

9. Claims 13-16 and 28-31 are rejected under 35 U.S.C. 103(a) as being obvious over Grisamore (U.S. 6,535,901) in view of Chang et al. ("Hardware-efficient implementations for discrete function transforms using LUT-based FPGAs") in view further of Fang et al. ("A hierarchical functional structuring and partitioning approach for multiple-FPGA implementations").

Re claims 13-16, Grisamore in view of Chang disclose in Figures 1, 4-5, and 7 an FPGA architecture to implement the one or more full-adders (Figure 3), half-adders (Figure 2), and single registers (col. 1 lines 35-40), the architecture based at least in part on an analysis of the input terms (col. 2 lines 35-40) comprising a bit-wise analysis (col. 2 lines 33-35). Grisamore does not disclose in Figures 1, 4-5, and 7 a controller or a logic control module dynamically structures the atomic elements of the

dedicated logic device. However, Fang et al. disclose in Figure 3 a controller or a logic control module dynamically (left column 3rd paragraph page 1189 and Module1(DP) in Figure 3) structures the atomic elements of the dedicated logic device (Figure 3). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a controller or a logic control module dynamically structures the atomic elements of the dedicated logic device as seen in Fang's invention into Grisamore in view of Chang's invention because it would enable an operator to dynamically program or configure a specific function in low manufacturing time and cost.

Re claim 28, it is a method claim of claim 13. Thus, claim 28 is also rejected under the same rationale in the rejection of rejected claim 13.

Re claim 29, it is a method claim of claim 14. Thus, claim 29 is also rejected under the same rationale in the rejection of rejected claim 14.

Re claim 30, it is a method claim of claim 16. Thus, claim 30 is also rejected under the same rationale in the rejection of rejected claim 16.

Re claim 31, it is a method claim of claim 15. Thus, claim 31 is also rejected under the same rationale in the rejection of rejected claim 15.

10. Claims 32, 36-38, and 42-43 are rejected under 35 U.S.C. 103(a) as being obvious over Grisamore (U.S. 6,535,901) in view of Greenberger (U.S. 6,411,979).

Re claim 32, Grisamore discloses in Figures 1, 4-5, and 7 a method for performing arithmetic comprising: generating a plurality of partial products from two or

more input terms(12); that implements in one or more full-adders, half-adders, and single registers to produce intermediate summation results by combining the partial products (col. 1 lines 35-40 and col. 2 lines 35-40); determining the structure of the Boolean function generators based, at least in part, on one or more attributes of the input terms (col. 8 lines 20-30); receiving in both branches accumulator bits over a feedback path (26 and 28); and adding (18) the intermediate summation results with the accumulator bits for each branch to produce a final real-component sum and a final imaginary-component sum. Grisamore does not implicitly disclose two paths one for a real-component branch, inverting certain partial products and passing the inverted and non-inverted partial products and one for an imaginary-component branch, passing the partial products to a multi-stage series of Boolean function generators simultaneously. However, Greenberger clearly discloses in page 2 a complex arithmetic operation comprising two paths (real and imaginary wherein label with Zr and Zi) one for a real-component branch (left side of Figure 2) inverting certain partial products (34.1) and passing the inverted and non-inverted partial products and one for an imaginary-component branch (right side of Figure 2), passing the partial products (34.2). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add two paths one for a real-component branch, inverting certain partial products and passing the inverted and non-inverted partial products and one for an imaginary-component branch, passing the partial products as seen in Greenberger's invention into Grisamore's invention because it would enable to reduce the complexity of processing the complex operands and increase the speed of operation.

Re claim 36, Grisamore further discloses in Figures 1, 4-5, and 7 generating a plurality of partial product terms comprises combining the two or more inputs in a combinatorial stage of a complex multiply accumulator (Figure 1).

Re claim 37, Grisamore further discloses in Figures 1, 4-5, and 7 analyzing one or more attributes of the input terms (col. 2 lines 35-40).

Re claim 38, it is a method claim of claim 15. Thus, claim 38 is also rejected under the same rationale in the rejection of rejected claim 15.

Re claim 42, Grisamore further discloses in Figures 1, 4-5, and 7 the multi-stage series of Boolean function generators are pipelined (Figure 5 wherein the reduction stage goes from high to low; e.g. 6, 4, 2...).

Re claim 43, Grisamore further discloses in Figures 1, 4-5, and 7 the partial products of the two or more input terms are reduced according to a pattern structured (col. 2 lines 35-43) by maximally partitioning bits of equal significance into groups of three to be passed as inputs to the full-adders, remaining groups of two to be passed ms inputs to the half-adders (col. 8 lines 20-30), and remaining single bits to be passed to single registers (col. 5 lines 48-53).

11. Claims 33-35 are rejected under 35 U.S.C. 103(a) as being obvious over Grisamore (U.S. 6,535,901) in view of Greenberger (U.S. 6,411,979), as applied to claim 32 above, in further view of Chang et al. ("Hardware-efficient implementations for discrete function transforms using LUT-based FPGAs").

Re claim 33, it has same limitations cited claim 10. Thus, claim 33 is also rejected under the same rationale in the rejection of rejected claim 10.

Re claim 34, it has same limitations cited claim 11. Thus, claim 34 is also rejected under the same rationale in the rejection of rejected claim 11.

Re claim 35, it has same limitations cited claim 12. Thus, claim 35 is also rejected under the same rationale in the rejection of rejected claim 12.

12. Claims 39-41 are rejected under 35 U.S.C. 103(a) as being obvious over Grisamore (U.S. 6,535,901) in view of Greenberger (U.S. 6,411,979) in further view of Chang et al. ("Hardware-efficient implementations for discrete function transforms using LUT-based FPGAs") and in further view of Fang et al. ("A hierarchical functional structuring and partitioning approach for multiple-FPGA implementations").

Re claim 39, it has same limitations cited claim 13. Thus, claim 39 is also rejected under the same rationale in the rejection of rejected claim 13.

Re claim 40, it has same limitations cited claim 14. Thus, claim 40 is also rejected under the same rationale in the rejection of rejected claim 14.

Re claim 41, it has same limitations cited claim 16. Thus, claim 41 is also rejected under the same rationale in the rejection of rejected claim 16.

Response to Arguments

13. Applicant's arguments filed 08/23/2004 have been fully considered but they are not persuasive.

a. The applicant argued in page 15 third paragraph for independent claims 2 and 17 that the cited reference by Grisamore does not disclose pipelined adder tree reduction stage wherein Grisamore does not include any registers between adders like those depicted.

The examiner respectfully submits that Grisamore disclose the pipelined adder tree reduction stage as cited in the present claims. First of all, Grisamore discloses in columns 2-3 under the detailed description of a preferred embodiment section a reduction tree module (Figures 1 and 5) for reducing the step and increase the multiply accumulation circuit (col. 2 lines 25-28) using certain arranged full adders, half-adders, and memory (col. 2 lines 35-43). Second, Grisamore further discloses in Figure 5 an example wherein the reduction stage is going through a series sub-stage (layer 6, 4, 3, 2) in pipeline one after another in Figure 5, larger number would go from higher layer down to layer 2. Third, Grisamore further discloses in column 5 lines 49-53 for those bits which do not need further reduction will copy to next layer until last layer (layer 2). Based on those cited reasons above, the cited reference by Grisamore does disclose pipelined adder tree reduction stage.

b. The applicant argued further in page 16 that Grisamore fails to disclose the reduction tree structured to maximally partition bits of equal significance into groups to three to serve as inputs to full-adders with remaining groups of two serving a s inputs to half-adders and remaining single bits as inputs to registers.

The examiner respectfully submits that these limitations are clearly cited in the rejection above wherein the input bits of equal significance are maximally partitioned into groups of three to serve as inputs to full-adders (col. 8 lines 20-33), remaining groups of two to serve as inputs to half-adders (col. 8 lines 20-33), and remaining single bits to serve as inputs to single registers (col. 5 lines 48-53). In addition, the applicant does not clearly define the boundary for maximum partition. Without further incorporate above rejection, Figure 5 clearly discloses the cited limitations wherein reduction from one layer to the next layers would need appropriated full-adder and half-adder (col. 8 lines 20-30).

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

November 26, 2004

TODD INGBERG
PRIMARY EXAMINER